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| **Title** | **Demonstrate and apply knowledge of digital systems technology** | | |
| **Level** | **5** | **Credits** | **15** |

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| **Purpose** | This unit standard covers aspects of digital systems from a basic level through to an intermediate level. It also covers aspects of how individual digital system components are integrated into complete systems.<br><br>People credited with this unit standard are able to demonstrate:<br>- knowledge of digital system building blocks;<br>- and apply knowledge of PLDs; and<br>- knowledge of digital interfacing techniques in accordance with industry practice. |

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| **Classification** | Electronic Engineering > Core Electronics |

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| **Available grade** | Achieved |

**Guidance Information**

1 This unit standard is intended for use in engineering courses at diploma level.

2 It is recommended that competency in Unit 22726, *Demonstrate and apply introductory knowledge of electronic engineering*; and Unit 22734, *Demonstrate and apply introductory knowledge of electrotechnology engineering mathematics;* be achieved before assessment against this unit standard is attempted, or equivalent knowledge and skills demonstrated.

3 Reference
Health and Safety in Employment Act 1992;
and all subsequent amendments and replacements.

4 Definitions
*a.c.*– alternating current.
*BCD* – binary coded decimal.
*d.c.* – direct current.
*Industry practice* – practice used and recommended by organisations involved in the electrotechnology industry.
*PLD* – programmable logic device.

5 All measurements are to be expressed in Système International (SI) units, and, where required, converted from Imperial units into SI units.

6 All activities must comply with: any policies, procedures, and requirements of the organisations involved; the standards of relevant professional bodies; and any relevant legislative and/or regulatory requirements.

7 Range
- a performance in relation to the elements of this unit standard must comply with the Health and Safety in Employment Act 1992;
- b laboratory and workshop safety practices are to be observed at all times.

## Outcomes and performance criteria

### Outcome 1

Demonstrate knowledge of digital system building blocks.

Range counters, shift registers, astable and monostable devices, Schmitt trigger, clock sources.

**Performance criteria**

1.1 The characteristics and concepts of digital system building blocks are described in accordance with industry practice.

1.2 Rules, logic, and formulae used in relation to digital system building blocks are explained in accordance with industry practice.

### Outcome 2

Demonstrate and apply knowledge of PLDs.

**Performance criteria**

2.1 The basic architecture of different types of PLDs and gate arrays are compared and explained in accordance with industry practice.

2.2 Applications for PLD designs are described.

2.3 PLD programs are created, compiled, and implemented in hardware devices to given specifications in accordance with industry practice.

Range may include but is not limited to – Boolean, state, schematic capture.
Evidence of three implemented programs is required.

2.4 Tests conducted in accordance with industry practice confirm that the program meets the given specification requirements.

### Outcome 3

Demonstrate knowledge of digital interfacing techniques.

**Performance criteria**

3.1 Transducer types, applications, construction, and input and output types are described, and interfacing requirements are explained in accordance with industry practice.

Range digital inputs – interfacing to switches, keypads, BCD switches, optical isolation;
digital outputs – interfacing to relays, heavy d.c. sink and source loads, optical isolators driving a.c. loads, H-bridges.

3.2 The interfacing circuitry between transducers and the inputs of digital devices is explained and implemented in accordance with industry practice.

Range evidence of two interfaces is required.

3.3 The interfacing circuitry between digital devices and output transducers is explained and implemented in accordance with industry practice.

Range evidence of two interfaces is required.

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**This unit standard is expiring. Assessment against the standard must take place by the last date for assessment set out below.**

**Status information and last date for assessment for superseded versions**

| Process | Version | Date | Last Date for Assessment |
|---|---|---|---|
| Registration | 1 | 27 April 2000 | 31 December 2024 |
| Review | 2 | 18 December 2006 | 31 December 2024 |
| Review | 3 | 24 August 2023 | 31 December 2024 |

| Consent and Moderation Requirements (CMR) reference | 0003 |
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This CMR can be accessed at http://www.nzqa.govt.nz/framework/search/index.do.