Title	**Demonstrate and apply fundamental knowledge of digital electronics for electronics technicians**		
Level	**3**	**Credits**	**7**

Purpose	This unit standard covers an introduction to digital electronic devices and circuits for electronics technicians. People credited with this unit standard are able to demonstrate: – knowledge of number systems; – knowledge of combinational logic circuits; – knowledge of TTL and CMOS logic families; – knowledge of simple sequential logic circuits; – and apply knowledge of PLDs; and – knowledge of integrated circuit pulse generators and timers.

Classification	Electronic Engineering > Core Electronics

Available grade	Achieved

Guidance Information

1 This unit standard has been developed for learning and assessment off-job.

2 References
Health and Safety in Employment Act 1992 and associated regulations;
and all subsequent amendments and replacements.

3 Definitions
Fundamental knowledge – for the purposes of this unit standard means having some relevant theoretical knowledge of the subject matter with the ability to use that knowledge to interpret available information.
CMOS – complementary metal oxide semiconductor.
Enterprise practice – those practices and procedures that have been promulgated by the company or enterprise for use by their employees.
Industry practice – those practices that competent practitioners within the industry recognise as current industry best practice.
PIPO – parallel in – parallel out.
PISO – parallel in – serial out.
PLD – programmable logic device.
SIPO – serial in – parallel out.
SISO – serial in – serial out.
TTL – transistor – transistor logic.

4 Range
- a Electrical, radiation, and workshop or laboratory safety practices are to be observed at all times.
- b All measurements are to be expressed in Système Internationale (SI) units and multipliers.
- c Use of non-programmable calculators is permitted during assessments.
- d All activities and evidence presented for all outcomes and performance criteria in this unit standard must be in accordance with legislation, policies, procedures, ethical codes, Standards, applicable site and enterprise practice, and industry practice; and, where appropriate, manufacturers' instructions, specifications, and data sheets.

Outcomes and performance criteria

Outcome 1

Demonstrate knowledge of number systems.

Performance criteria

1.1 Signed and unsigned numbers are converted to and from the decimal number system to binary, hexadecimal, and binary coded decimal.

Range maximum of 8 bit binary and 4 digit hexadecimal numbers.

1.2 Binary numbers are added and subtracted.

Range evidence of twenty different additions and twenty different subtractions is required.

1.3 Special binary code formats are described.

Range may include but is not limited to – 8421, ASCII, BCD to seven segment, Gray code;
evidence of two codes is required.

Outcome 2

Demonstrate knowledge of combinational logic circuits.

Range maximum of 10 gates and limited to three variables.

Performance criteria

2.1 Boolean expression is obtained from a given logic diagram and truth table.

2.2 Logic diagram is drawn from Boolean expression.

2.3 Boolean expression is simplified using simple Boolean algebra identities and/or Karnaugh maps.

2.4 Logic diagrams are converted to and from NAND and NOR logic.

Outcome 3

Demonstrate knowledge of TTL and CMOS logic families.

Performance criteria

3.1 Logic switching voltage thresholds are compared.

3.2 Common logic parameters are described.

Range power supply requirements, sink and source capabilities.

3.3 Handling precautions when using TTL and CMOS components are explained.

Outcome 4

Demonstrate knowledge of simple sequential logic circuits.

Performance criteria

4.1 Simple latch operation is described using truth tables.

Range may include but is not limited to – S-R flip-flop using gates, J-K, D types.

4.2 Circuits for asynchronous up-counters and down-counters are drawn and their operation explained.

Range asynchronous modulus 10, modulus 16.

4.3 Circuits for simple shift registers are drawn and explained.

Range may include – SISO, PIPO, PISO, SIPO, one direction using D flip-flops;
evidence of two is required.

4.4 The difference between level and edge triggering is explained.

Outcome 5

Demonstrate and apply knowledge of PLDs.

Performance criteria

5.1 The basic architecture of different types of PLDs and gate arrays are compared.

5.2 Simple PLD programs are created, compiled, and one of which is implemented in hardware devices to a given Boolean expression or logic diagram.

Outcome 6

Demonstrate knowledge of integrated circuit pulse generators and timers.

Range astable, monostable, timer circuits.

Performance criteria

6.1 Circuits are identified from given circuit diagrams, and their operation described with reference to the function of each major component.

6.2 One practical application of each pulse generator and timer is described.

This unit standard is expiring. Assessment against the standard must take place by the last date for assessment set out below.

Status information and last date for assessment for superseded versions

Process	Version	Date	Last Date for Assessment
Registration	1	24 November 2003	31 December 2011
Rollover and Revision	2	22 August 2008	31 December 2012
Review	3	21 July 2011	31 December 2024
Review	4	25 May 2023	31 December 2024

Consent and Moderation Requirements (CMR) reference	0003

This CMR can be accessed at http://www.nzqa.govt.nz/framework/search/index.do.